III. REMARKS

1. Claims 1-15 and 17-26 remain in the application. Claim 16 has been cancelled without prejudice. Claims 1, 13-15, 21, 25, and 26 have been amended.

Support for the amendments may be found in the specification, for example, on page 26, line 23 through page 27, line 22, and in Figure 8.

2. Applicants respectfully submit that claims 17, 19, 21, and 23 are definite under 35 USC 112, second paragraph. These claims are directed to a testing system for testing at least one of a first and second unit to be tested. The first and second units are designated as units to be tested, and the system is for testing at least one of the designated units. The claims do not describe a system that is required to test both units, only for testing at least one of the units.

3. Applicants respectfully submit that claims 1-6, 8, 11-14, 17 and 18 are not anticipated by Magoshi (US 5,886,901) under 35 USC 102(b).

3.1 Magoshi fails to disclose or suggest that the coupling unit includes a second signal path for providing a signal connection between the at least one terminal of the second unit to be tested and the at least one terminal of the first unit to be tested, and also fails to disclose or suggest switching facilities adapted for switching the signal path so as to select a signal of the first signal path or the second signal path, as recited by claim 1.

Claim 1 is directed to parameterized loop back testing as applied to bidirectional interfaces as shown in Fig. 8. This embodiment provides for a first signal connection 832 for signal transfer from a first unit to a second unit and a second signal connection 842 for signal transfer from a second unit to a first unit.

Magoshi relates to specific implementations of flip-flops for a scan test chain for testing combinational logic, wherein a scan test chain (comprising flip-flop cells 200, 220, 240) for testing combinational logic 260 is shown in Fig. 2 of Magoshi. During normal operation, the flip-flop cells receive input data from data input lines 202, 222 and 224, i.e. data output from the combinational logic 260. The flip-flop cells output data on output terminals 210, 230, 250, wherein the combinational logic 260 receives those data output from the output terminals 210, 230 and 250 at respective inputs thereof (see column 5, lines 37 to 48 of Magoshi, for example).

During a test mode, the data inputs 202, 222 and 242 of the flip-flop cells are de-asserted and test inputs TI are asserted. Accordingly, the flip-flop cells act as a shift register and data can serially be shifted through the flip-flop cells without passing the combinational logic 260. In order to avoid timing violations in the test mode (in which data shifted from flip-flop cell to flip-flop cell), delay elements are provided between or within the flip-flop cells in the scan test chain (see 410 in Fig. 4, 500 in Fig. 5, 600 in Fig. 6 and 720 in Fig. 7).

Testing using such a scan test chain is performed as follows. Known data is serially shifted into the flip-flop cells through

the serial scan chain. Once the data is in place, the output pins of the combinational logics are sampled (read into the flip-flop cells). Thereupon, the data from the flip-flop cells are serially shifted to the scan chain output and are compared to an expected output (see column 1, lines 15 to 24 of Magoshi).

According to Magoshi, a single signal path is provided between the outputs of the combinational logic (connected to the data input terminals 202, 222, 242 of the flip-flop cells) and the inputs of the combinational logic (connected to the output terminals 210, 230 and 250).

Magoshi is clearly silent about a first signal path and a second signal path between two units to be tested. It is also clear that Magoshi is silent about switching facilities, both features as taught by claim 1.

The first paragraph on page 9 of the present Office Action states that Magoshi substantially teaches a second signal path that is adapted to provide a signal connection between the at least one terminal of the second unit to be tested and the at least one terminal of the first unit to be tested. The U.S. Examiner refers to Fig. 2 and column 6, lines 2 to 50. However, as explained above, neither Fig. 2 nor column 6, lines 2 to 50 teach two signal paths between the respective outputs and inputs of the combinational logic. Accordingly, Magoshi clearly does not teach a first signal path and a second signal path between two circuit units to be tested.

The first paragraph on page 9 of the present Office Action also refers to the delay element 720 shown in Fig. 7 of Magoshi. According to Fig. 7, the delay element 720 is provided following the data storage element 130 while, according to Figures 5 and

6, the delay elements 500 and 600, respectively are provided preceding the data storage element 130. Therefore, the delay element 720 is not provided in addition to the delay elements 500 and 600, respectively, but actually replaces same. Accordingly, Magoshi clearly does not include any teaching as to two data paths comprising signal conditioning facilities between a first unit to be tested and a second unit to be tested.

As explained above, Magoshi relates to a scan test chain for performing serial scan tests. The cited prior art does not include any hint that would motivate a person skilled in the art to modify the system of Magoshi such that he would obtain what is claimed in the present application. Moreover, the prior art is silent about any hint as to how such a modification could look like. In particular, there is no hint as to how a second signal path could be implemented along with the serial scan chain disclosed in Magoshi.

At least for these reasons, Applicants submit that Magoshi does not anticipate independent claim 1 and dependent claims 5, 6, 8, 11-14, 17, and 18.

4. Applicants respectfully submit that claims 7, 9, 10, 15, 16, 19 and 20-26 are patentable over Magoshi under 35 USC 103(a).

4.1 Claims 7, 9, 10, 15, 16, 19, and 20 depend from claim 1.

As argued above, Magoshi fails to disclose or suggest that the coupling unit includes a second signal path for providing a signal connection between the at least one terminal of the second unit to be tested and the at least one terminal of the first unit to be tested, and also fails to disclose or suggest

switching facilities adapted for switching the signal path so as to select a signal of the first signal path or the second signal path, as recited by claim 1.

Therefore, claims 7, 9, 10, 15, 16, 19 and 20 are patentable over Magoshi.

4.2 Magoshi also fails to disclose or suggest receiving a second signal from the second unit to be tested, conditioning the second signal in accordance with predefined parameters and providing the conditioned second signal as a second input signal to the first unit to be tested, as recited by claim 21.

As mentioned above, Magoshi only provides a single signal path between the outputs of the combinational logic connected to the data input terminals 202, 222, 242 and the inputs of the combinational logic connected to the output terminals 210, 230 and 250.

Claims 22-26 depend from claim 21 and therefore claims 21-26 are not rendered obvious by Magoshi.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record, and are in proper form for allowance. Accordingly, favorable reconsideration and allowance is respectfully requested. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

The Commissioner is hereby authorized to charge payment for any fees associated with this communication or credit any over payment to Deposit Account No. 16-1350.

Respectfully submitted,

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